



Creating Assertion-Based IP (Integrated Circuits and Systems)

Harry D. Foster, Adam C. Krolnik

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This book presents formal testplanning guidelines with examples focused on creating assertion-based verification IP. It demonstrates a systematic process for formal specification and formal testplanning, and also demonstrates effective use of assertions languages beyond the traditional language construct discussions

Note that there many books published on assertion languages (such as SystemVerilog assertions and PSL). Yet, none of them discuss the important process of testplanning and using these languages to create verification IP. This is the first book published on this subject.

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